IN THE CLAIMS:

Claims 1-7 (canceled)

8. (Currently Amended) A semiconductor substrate comprising:

a trench region comprising at least one trench, said trench comprising a single layer of ~~seamless~~ doped high-density plasma (HDP) ~~HDP~~ oxide having an unpolished upper surface; and

a non-trench region having an upper surface which is substantially co-planar with said unpolished upper surface of said single layer of said ~~seamless~~ HDP oxide,

~~wherein said upper surface of said HDP oxide and said upper surface of said non-trench region are planarized without etch-back~~.

Claims 9-14 (canceled)

15. (Currently Amended) A semiconductor substrate comprising:

a trench region comprising a plurality of trenches, each of said trenches comprising a single layer of doped ~~seamless~~ high density plasma (HDP) oxide having an unpolished upper surface; and

a non-trench region having an upper surface which is substantially co-planar with said unpolished upper surface of said single layer of said seamless HDP oxide,

wherein said upper surface of said non-trench region comprises implanted dopants; ~~and~~

~~wherein said upper surface of said HDP oxide and said upper surface of said non-trench region are planarized without etch-back~~.

Claims 16-22 (canceled)

23. (Currently Amended) A semiconductor substrate comprising:

a trench region comprising at least one wide trench and at least one narrow trench a

~~plurality of trenches~~, each of said trenches comprising a single layer of doped ~~seamless~~ high density plasma (HDP) oxide having an unpolished upper surface; and

a non-trench region having an upper surface which is substantially co-planar with said unpolished upper surface of said single layer of said seamless HDP oxide,

wherein said upper surface of said non-trench region comprises implanted dopants; ~~and~~

~~wherein said upper surface of said HDP oxide and said upper surface of said non-trench region are planarized without etch-back~~.

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24. (Previously presented) The semiconductor substrate according to claim 8, wherein said high density plasma oxide comprises non-conformal high density plasma oxide.

25. (Previously presented) The semiconductor substrate according to claim 8, wherein said at least one trench comprises at least one wide trench and at least one narrow trench.

26. (Currently amended) The semiconductor substrate according to claim 8, wherein said doped high density plasma oxide comprises fluorine-doped high density plasma oxide ~~a low dielectric constant oxide~~.

27. (Previously presented) The semiconductor substrate according to claim 1, wherein said high density plasma oxide comprises silicon dioxide.

28. (Currently amended) The semiconductor substrate according to claim 24, wherein said high density plasma oxide comprises silicon dioxide doped with ~~one of phosphorus, boron and~~ fluorine.

29. (Previously presented) The semiconductor substrate according to claim 8, wherein said surface of said filler material and said surface of said substrate are planarized without reactive ion etching.

30. (Previously presented) The semiconductor substrate according to claim 8, wherein said at least one trench comprises shallow trench isolations.

31. (Currently amended) The semiconductor substrate according to claim 8, wherein said upper surface of said single layer of ~~seamless~~ HDP oxide and said upper surface of said non-trench region are planarized without chemical mechanical polishing.

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32. (Currently amended) The semiconductor substrate according to claim 8, wherein said upper surface of said single layer of ~~seamless~~ HDP oxide is substantially scratch-free.

33. (Currently amended) The semiconductor substrate according to claim 8, wherein said surface of said non-trench region ~~substrate~~ comprises implanted dopants.

34. (Previously presented) The semiconductor substrate according to claim 8, further comprising:

a thin oxide layer grown on said upper surface of said substrate.

35. (Currently amended) The semiconductor substrate according to claim 8, wherein said upper surface of said single layer of ~~seamless~~ HDP oxide is free of chatter marks.

36. (Currently amended) The semiconductor substrate according to claim 23, wherein said ~~at least one trench comprises~~ at least one wide trench is formed adjacent to said ~~and~~ at least one narrow trench.

37. (Currently amended) The semiconductor substrate according to claim 23, wherein said doped HDP oxide comprises fluorine-doped HDP oxide ~~implanted dopants comprise at least one of phosphorus, boron and fluorine~~.

38. (Previously presented) The semiconductor substrate according to claim 23, wherein

said high density plasma (HDP) oxide comprises non-conformal HDP oxide.

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39. (New) The semiconductor substrate according to claim 37, further comprising:

a thin oxide layer grown on said upper surface of said substrate, said thin oxide layer comprises a high-purity oxide.

40. (New) The semiconductor substrate according to claim 8, wherein a thickness of said single layer of HDP oxide comprises an as-deposited thickness.